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Reducing Leakage Currents in n-Channel Organic Field-Effect Transistors Using Molecular Dipole Monolayers on Nanoscale Oxides

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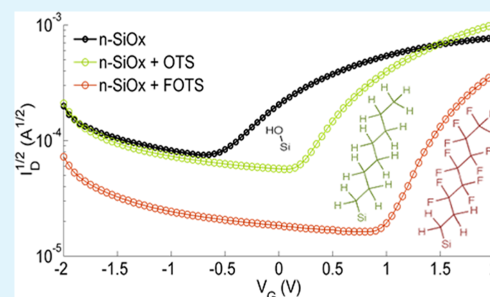
Supporting Information

ABSTRACT: Leakage currents through the gate dielectric of thin film transistors remain a roadblock to the fabrication of organic field-effect transistors (OFETs) on ultrathin dielectrics. We report the first investigation of a self-assembled monolayer (SAM) dipole as an electrostatic barrier to reduce leakage currents in n-channel OFETs fabricated on a minimal, leaky ~10 nm SiO_2 dielectric on highly doped Si. The electric field associated with 1*H*,1*H*,2*H*,2*H*-perfluoro-octyltriethoxysilane (FOTS) and octyltriethoxysilane (OTS) dipolar chains affixed to the oxide surface of n-Si gave an order of magnitude decrease in gate leakage current and subthreshold leakage and a two order-of-magnitude increase in ON/OFF ratio for a naphthalenetetracarboxylic diimide (NTCDI) transistor. Identically fabricated devices on p-Si showed similarly reduced leakage and improved performance for oxides treated with the larger dipole FOTS monolayer, while OTS devices showed poorer transfer characteristics than those on bare oxide. Comparison of OFETs on both substrates revealed that relative device performance from OTS and FOTS treatments was dictated primarily by the organosilane chain and not the underlying siloxane−substrate bond. This conclusion is supported by the similar threshold voltages (V_T) extrapolated for SAM-treated devices, which display positive relative V_T shifts for FOTS on either substrate but opposite V_T shifts for OTS treatment on n-Si and p-Si. Our results highlight the potential of dipolar SAMs as performance-enhancing layers for marginal quality dielectrics, broadening the material spectrum for low power, ultrathin organic electronics.



KEYWORDS: *organic field-effect transistor, monolayer, dielectric, interface dipole, threshold voltage, leakage current*

INTRODUCTION

Organic field-effect transistors (OFETs) are often touted as flexible, low-cost alternatives to silicon technology where the device area needs not to be microscopic. Applications where OFET circuitry might be useful, such as in mass produced displays,[1,2] radio frequency identification tags,[3,4] and sensors,[5,6] often require that power consumption and input voltage be minimized. However, the typical OFET test architecture, the organic semiconductor (OSC) film on 100−300 nm of SiO_2 deposited on a conductive Si gate with >100 μm spacing between source and drain electrodes, requires tens of volts to achieve effective switching. In the past decade, many groups have studied high-capacitance dielectric layers in order to decrease operating voltages and enable closer source-drain separations than are typical for Si-SiO_2 substrates.[7] They used very thin amorphous polymers,[8] monolayer-treated[9−12] or polymer-treated inorganic dielectrics,[13] polymer electrolyte dielectrics,[14] and high-k inorganic dielectrics.[15] An ultimate solution would be to produce OFETs from single layers of molecules that include both a dielectric side chain and a conjugated subunit; this has been attempted previously,[16,17] and we have recently reported the first demonstration of OSC molecular segments within a multilayer film contributing to gate capacitance, acting substantially as gate materials in series with very thin oxide films.[18] Still, the apparently insufficient dielectric strength in those devices allowed considerable gate leakage current and limited the ON/OFF ratio. It is not known whether this leakage was the result of pinhole defects in the oxides or dielectric breakdown.

Although flexible substrates with a variety of metal/dielectric systems have been developed for organic electronics applications, the Si−SiO_2 platform remains attractive for organic semiconductor device testing and characterization because of its flatness, standardization, and relatively dense oxide coverage compared to alternative ultrathin dielectric films on metals. Another advantage is the ability to functionalize the

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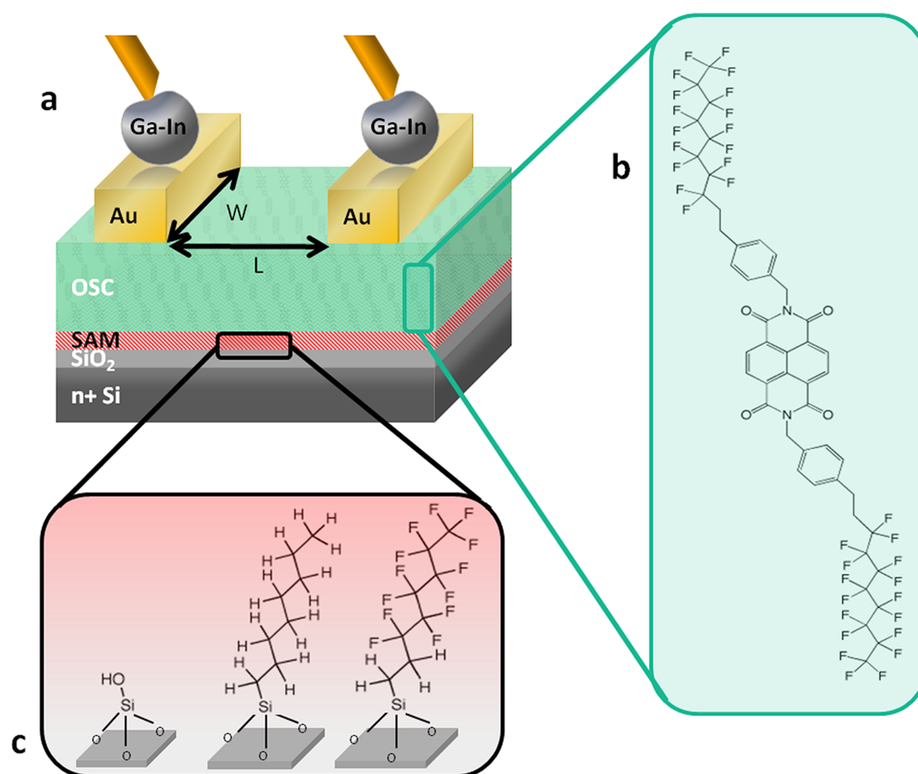

Figure 1. Experimental platform for probing the effect of a molecular dipole. (a) OFET fabricated on a plasma-grown 10 nm minimal oxide with a SAM at the dielectric/OSC interface. (b) Chemical structure of 8-2-Bn NTCDI. (c) Bare oxide and SAM-functionalized oxide with OTS and FOTS.

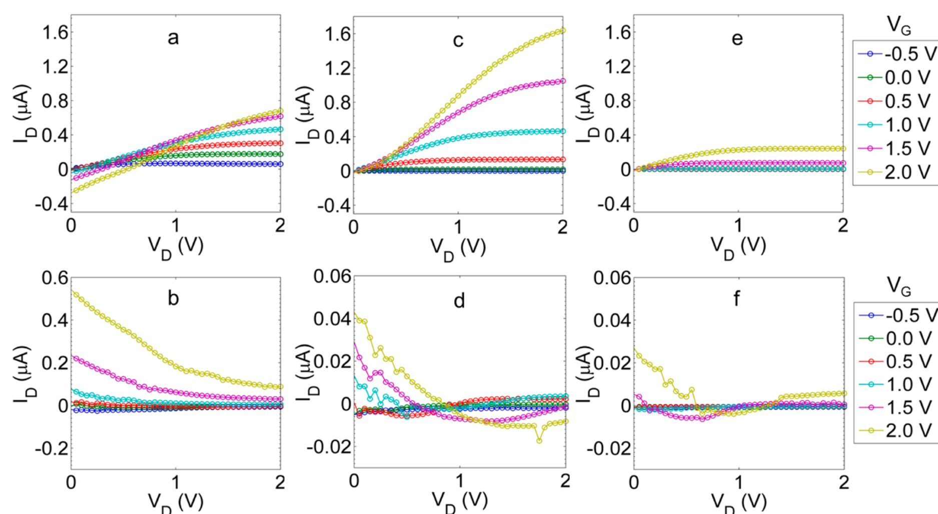

Figure 2. Output (top panels) and leakage (bottom panels) characteristics of 8-2-Bn NTCDI OFETs fabricated on highly doped n-type silicon with 10 nm plasma-grown oxide. (a, b) Devices on bare oxide. (c, d) Devices on OTS. (e, f) Devices on FOTS. Each curve is of data from averages of three devices on the same substrate for each wafer type. Device W/L ratio is 53.3. Note that the scale for (b) is 10× the scale for (d) and (f).

oxide surfaces with monolayers that can tune surface energy and local electric fields. When degenerately doped, Si is sufficiently conductive to allow easy equilibration of remotely applied gate voltages (V_G) with arrays of OFETs. However, on the basis of our previous observations, thin oxides grown from highly doped wafers yield less-insulating dielectrics than do thicker or chemical vapor-deposited SiO_2. High gate leakage has a detrimental effect on transistor performance, resulting in high OFF currents, low ON/OFF ratios, and increased power consumption, all of which negate the potential advantages of low-power OSC-based electronics. As a result, reducing the gate leakage in thin bottom gate-top contact OFETs is a technological priority for the study and development of OSC-based devices. In this paper, we discuss the use of dipolar silane self-assembled monolayers (SAMs) to reduce the gate leakage in a thin-oxide OFET fabricated on highly doped silicon, as illustrated in Figure 1. While other examples of SAMs used to shift OFET threshold voltages (V_T) have been reported by us and others,[19−21] this is the first study of a SAM dipole being used specifically to lower gate leakage current. We employed two organosilanes, octyltriethoxysilane (OTS) and 1*H*,1*H*,2*H*,2*H*-perfluoro-octyltriethoxysilane (FOTS), with cal-

Table 1. Leakage Currents in n-Channel NTCDI OFETs on Bare and SAM-Teated n-Si and p-Si Oxides[a]

OFET dielectric (nA)	I_G − ON	I_G − OFF (V_G = 0 V)	I_G − OFF (V_G = −0.5 V)	I_D − OFF[b]	I_D − OFF[c]
n-SiOx	88	−2.9	−6.1	176	479
n-SiOx + OTS	−3.7	−0.3	−1.9	17.5	3.5
n-SiOx + FOTS	5.7	−0.5	−0.7	0.4	0.4
p-SiOx	7.2	−1.5	−1.5	0.2	1.1
p-SiOx + OTS	−7.1	−1.2	−1.4	2.1	5.4
p-SiOx + FOTS	3.5	−0.4	−0.7	0.3	0.2

[a] I_G currents are gate leakage under several biasing conditions. [b] OFF drain current measured from I_D−V_D curves. [c] OFF drain current measured from I_D−V_G curves.

culated gas-phase dipoles[22] of −0.31 and −3.49 D, respectively. An explicit contribution of the SAM dipole to the lowering of this current is demonstrated. We chose to work with an electron-transporting OSC, namely, 8-2-Bn naphthalenetetracarboxylic diimide (NTCDI, Figure 1b), to further bolster our understanding of this class of compounds, as they are particularly crucial for complementary organic logic circuits.[23−25] We also noted a surprising difference in the effect of one of the silanes on n-Si versus p-Si oxides. Conclusions drawn from this work will be applicable to dielectric films made from other materials with nanoscale thicknesses, including other metal-oxide combinations and polymers, which have been recently shown to be amenable to work function tuning by surface modification with SAMs.[26]

RESULTS AND DISCUSSION

Device Performance. Typical output curves of OFETs on thin plasma-grown oxides are shown in Figure 2. Devices were fabricated in four separate experiments with 8-2-Bn, and device performance was reproducible and consistent with what is presented herein. In addition, OFETs fabricated with 8-0-Bn, a shorter NTCDI moiety with no CH_2 groups between the fluorocarbon and phenyl groups,[18] displayed similar trends in output and leakage. Devices with different W/L ratios exhibit similar trends as those reported here for W/L = 53.3. Bare n-Si oxide devices exhibit gate leakage currents of 88 nA with a 2 V potential between gate and source terminals. Taking the area through which the source-gate current flows to be the area of one electrode and half of the channel and a thickness of 10 nm for the oxide, these values correspond to leakage current densities of 2.6 μA cm^{-2} at 2 MV cm^{-1}. While these leakage currents and electric fields are below those expected for dielectric breakdown, this relatively high leakage may be the result of tunneling across the oxide, possibly enhanced by the high concentration of dopant atoms within the oxide and at the Si/oxide interface.[27] The leakage currents in the ON state are roughly an order of magnitude lower than the ON currents, indicating that the ON current is primarily lateral, even with this minimal dielectric. The gate leakage currents (I_G) at zero drain voltage (V_D = 0, intercept of the curves with the vertical axis) are reliable values because at that biasing condition V_D = V_S, and therefore, the lateral OFF current is zero. The value of I_G when V_D = 2 V is complicated by the difference in electrode-gate potentials near the source and drain, respectively, and by possible charging currents. Notably, the bare oxide devices did not show saturation with V_G at 2 V, though we will see shortly that the SAMs enabled saturation under this condition.

Addition of OTS and FOTS at the n-Si-oxide/NTCDI interface has a significant effect on device output and gate leakage currents, as seen in Figure 2c−f. Relative to the bare oxide, OTS treatment results in increased output current, while addition of FOTS decreases output current. Experiments on p-type silicon (Figure S1, Supporting Information) show a similar trend in output current, though leakage current is observed to increase slightly for OTS devices, to be discussed later. The trends for both output and leakage in n- and p-type silicon were observed in numerous iterations of this experiment. The FOTS trend was also observed on devices fabricated on 100 nm thermally grown SiO_2 (Figure S2, Supporting Information). One factor that could have accounted for these OFET performance differences is the quality of the first few OSC layers,[28] where most of the field-accumulated charge resides in the OFET channel.[29] Images of NTCDI films of 40 nm thickness captured with AFM show similar morphology on the three kinds of dielectric surfaces (Figure S3, Supporting Information). However, 40 nm corresponds to approximately 11 monolayers of 8-2-Bn NTCDI, raising the possibility that AFM is portraying a morphology not exactly indicative of the dielectric interface.[30] To ascertain how much the SAM treatments influenced the growth and morphology of the bottom-most layers, samples with 15 nm (~4 monolayers) of NTCDI were vacuum deposited. AFM images (Figure S4, Supporting Information) show bare oxide and FOTS surfaces leading to similar NTCDI domains, whereas OTS surfaces resulted in slightly larger NTCDI grains, consistent with observations reported elsewhere for OSCs on OTS-treated surfaces.[31] It is likely that the greater connectivity of the NTCDI on OTS-treated oxide is responsible for the larger output current in our OTS transistors.

The addition of SAMs to the n-Si-oxide surface results in a substantial reduction in leakage for both OTS and FOTS devices. Comparison of Figures 2b, d, and f indicates that FOTS-treated OFETs display weaker gate voltage dependence of gate leakage than either bare oxide or OTS-treated devices. To elucidate leakage current details, we consider four device operation regimes representative of electronic logic biasing (Table 1). Hereafter, the ON state refers to the regime where the gate voltage is high (V_G = 2 V). The source voltage is always grounded (0 V), and the drain voltage V_D is held at 2 V. The first leakage current we examine is the ON state gate leakage, which arises from the source-gate potential difference. Both OTS and FOTS decrease the ON gate leakage by 15−20× as compared to bare oxide devices. The second leakage current of interest is the case where V_G is 0 V, where the effective bias is between the drain electrode and the gate; this biasing condition is the reverse of that for the ON state gate leakage. As compared to bare oxide, both SAM treatments result in a comparable 6× reduction in OFF state gate leakage. The similar leakage reduction in the ON state for both SAM treatments suggests this leakage is reduced simply by the addition of dielectric material to the total gate thickness. We also examined the gate leakage with a small negative gate

voltage. Under this biasing, OTS treatment reduces leakage by a factor of 3, whereas FOTS reduces this leakage by nearly 1 order of magnitude. The observation of only a marginal increase in the gate leakage for FOTS devices as a result of changing the gate voltage from 0 to −0.5 V, compared to a 6× increase for OTS devices, is consistent with the effect of a larger dipole on FOTS limiting the flow of electrons from gate to drain. Similar magnitudes and trends in leakage current were observed in n-SiOx-Au diode structures. Finally, we investigate the subthreshold drain leakage, which is the drain current in the V_G = 0 V state and is a combination of source-drain and gate-drain currents. Subthreshold leakage is reduced by an order of magnitude with OTS and by more than 400 times with FOTS. This leakage reduction for FOTS is remarkable considering that ON output currents for these OFETs were fully half of that of bare oxide devices. This effect has never been explicitly utilized to enable and enhance low-voltage OFET switching.

Threshold Voltage Shifts. Surface treatments with OTS and FOTS also result in noticeable (and for FOTS, expected) shifts in the threshold voltage V_T, as shown in Figure 3.

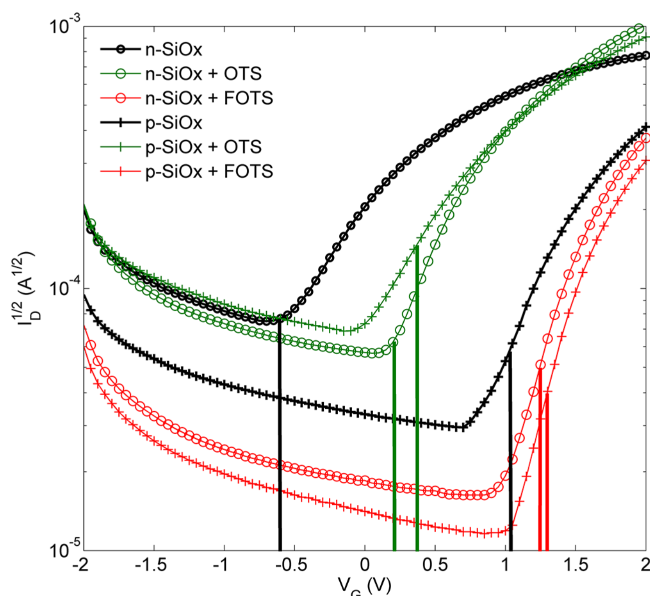

Figure 3. Effect of a molecular dipole on subthreshold leakage. $I_D^{1/2}$ vs V_G plot for OFETs with bare oxide, OTS, and FOTS on n-Si and p-Si. Vertical lines for bare oxide (black), OTS-treated (green), and FOTS treated (red) OFETs show threshold voltages. These voltages are similar for SAM-treated OFETs on each of the two substrates.

Threshold voltages were extrapolated from square-root transfer curves, over a linear region of 0.5 V above the turn-ON voltage. This method ensured that the extrapolated threshold voltage was not influenced by contact resistance at higher voltages, where the slope of the plot deviated from linearity. Bare oxide OFETs on n-Si displayed V_T = −0.58 V, while V_T = +0.21 V for OTS, and V_T = +1.25 V for FOTS. These data indicate that addition of SAMs at the n-Si/dielectric interface turns devices more OFF and suggest that the lower subthreshold leakage in SAM-treated devices is related to this threshold voltage tuning. The increase in V_T and decrease in ON output current for FOTS devices is consistent with this interpretation. Figure 3 shows that although OTS devices turn ON at more positive voltages, their subthreshold leakage in the depletion regime (V_G < 0) is nearly identical to that of bare oxide. By comparison, FOTS devices have an order of magnitude lower subthreshold leakage. It is possible that the marginally better quality of the NTCDI film on OTS may result in a greater number of mobile carriers at the OSC/dielectric interface, negating the effects of the OTS dipole. Nevertheless, there appears to be a net effect of the larger FOTS dipole on the leakage characteristics of our n-channel OFETs.

The trend established for n-Si devices alone would suggest that the greater magnitude of the FOTS dipole results in a larger threshold voltage shift versus bare oxide than does OTS but in the same direction. However, OFETs on p-SiOx display threshold voltages for bare oxide (V_T = +1.03 V) that are between OTS-treated (V_T = +0.24 V) and FOTS-treated (V_T = +1.29 V) oxides. The effects of OTS on gate leakage current are also different for p-SiOx compared to n-SiOx. To understand why the OTS dipole effects for p-SiOx differ from that observed for n-SiOx, we first address the differences between the bare oxide surfaces. The difference in turn-ON voltages for our OFETs on n-Si and p-Si devices of roughly 1.5 V arises from their respective Fermi level alignment with the top Au (source/drain) electrode in the MIS cross-section of the OFET device. This shift, though slightly larger, is in reasonable agreement with recent results from Yaffe et al.,[32] in which a 1.1 V difference between highly doped n- and p-Si diodes with a single alkyl SAM as a dielectric was observed.

Qualitatively, the discrepancy in the direction of the V_T shift (and the difference in effects on leakage current) for devices fabricated on SAM-treated n-SiOx and p-SiOx appears at odds with the notion that a surface-attached molecule acts purely as an electrostatic dipole; under that assumption, we would have expected OTS to also shift the V_T of devices on p-SiOx more positively. Instead, Figure 3 shows that devices made on both OTS- and FOTS-treated SiOx display very similar switching characteristics regardless of whether the underlying substrate is n-Si or p-Si. These data appear to suggest that a factor other than the silane-chain dipole makes an additional contribution to SAM-induced V_T shifts. We hypothesize that the SiOx-organosilane bonding itself makes a separate contribution to

Table 2. Comparison of OFET Device Parameters for Bare and SAM-Treated Oxides[a]

surface	V_T (V)	$S_{s\text{-th}}$ (mV/dec)	$\mu C/A$ (10^{-9} S/V)	μ_{meas} (10^{-2} cm^2/(Vs))	C_i (nF/cm^2)	ON/OFF (from V_{to})
n-SiOx	−0.58 ± 0.12	1480	4.4 ± 0.3	2.1 ± 1.0	192 ± 17	106
n-SiOx + OTS	+0.21 ± 0.03	607	9.4 ± 0.4	4.7 ± 1.9	131 ± 53	303
n-SiOx + FOTS	+1.25 ± 0.04	230	9.0 ± 0.6	4.5 ± 2.5	103 ± 16	460
p-SiOx	+1.03 ± 0.11	360	9.1 ± 3.6	3.0 ± 1.6	188 ± 5	208
p-SiOx + OTS	+0.36 ± 0.06	544	11.0 ± 3.7	3.9 ± 1.3	149 ± 4	175
p-SiOx + FOTS	+1.29 ± 0.09	226	9.5 ± 4.4	3.3 ± 2.1	141 ± 3	673

[a]Threshold voltages, mobility μ_{meas}, and sheet transconductance values were extrapolated from $I_D^{1/2}$ vs. V_G plots. Specific capacitance was measured at 100 Hz, using an electrode area of 3.03 × 10^{-2} cm^2. ON/OFF ratios were measured from V_{to} to 2 V. Device W/L ratio is 53.3.

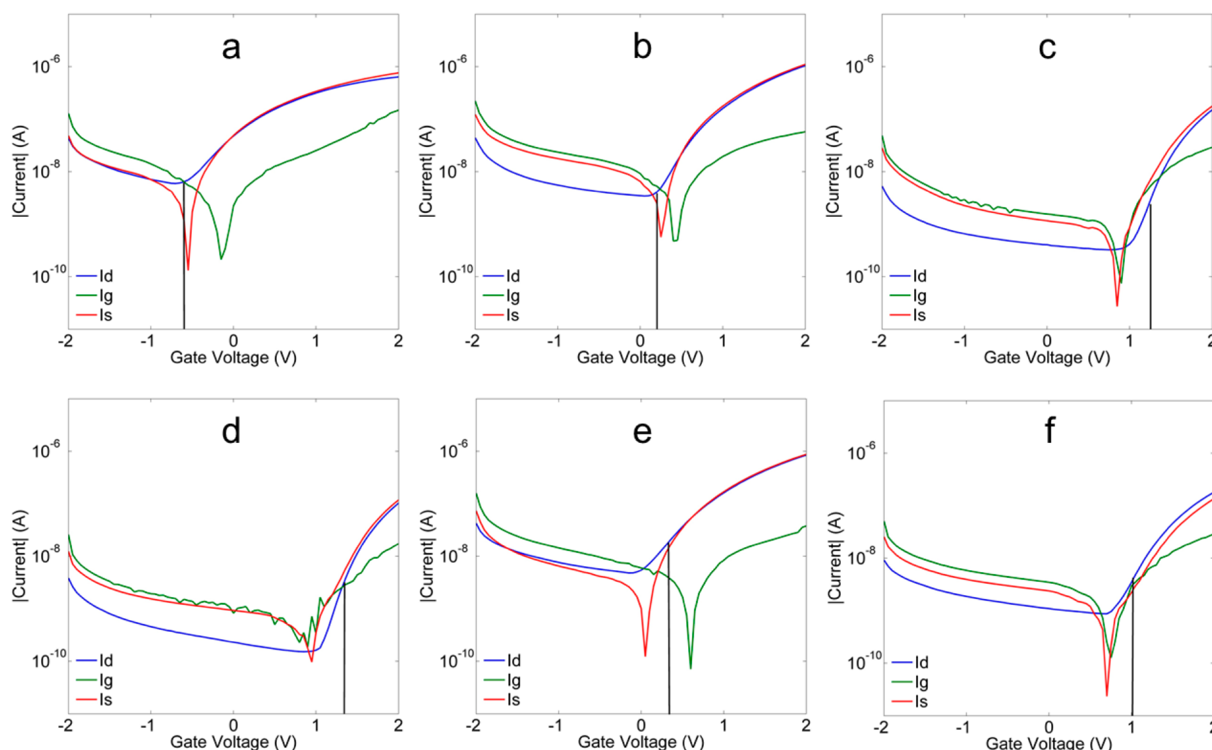

Figure 4. Terminal currents for high-leakage OFETs on n-SiOx (top panels) and p-SiOx (bottom panels). (a−c) Devices on bare, OTS-, and FOTS-treated n-Si oxide, respectively. (d−f) Devices on bare, OTS-, and FOTS-treated p-Si oxide. Vertical lines indicate the V_T as listed in Table 2.

the silane-induced surface dipole and that this contribution is different for OTS on n-Si and p-Si, while the contribution of the in-chain dipole of FOTS is similar on both oxides.

Finally, we attempted Kelvin-probe microscopy (SKPM) experiments to measure the surface potential differences between bare and SAM-treated oxides. We observed potential differences of −150 to −200 mV for both OTS and FOTS surfaces relative to both n-SiOx and p-SiOx, though the uncertainties among them were on the order of 100 mV, likely due to differences in humidity or surface contamination in our open-air system. The sign of this voltage, which we obtained in three separate experiments including different surface preparation processes (as explained in the Experimental Section), would be consistent with the effects of the silanes, except for the exceptional case of OTS on p-Si, where the silane-oxide bonding contribution may be somehow compensated in the SKPM experiment. A vacuum SKPM study performed with the NTCDI layer deposited on the substrates will be the topic of a future investigation of the SAM-OSC interfacial dipole.

Switching Behavior. Devices treated with OTS and FOTS show *much better switching characteristics* than devices on bare oxide, as evidenced by their improved subthreshold swing ($S_{s\text{-}th} = \partial V_G/\partial \ln I_D$) and reduced gate leakage. Table 2 summarizes these results for three devices on each surface treatment; sets of devices with smaller W/L ratios, all fabricated in parallel, exhibited similarly dampened gate leakage and switching characteristics effected by dipolar SAMs. As seen in Figure 3, the subthreshold swing $S_{s\text{-}th}$ for FOTS-treated devices is more than 1200 mV/dec lower than for bare oxide devices and more than 700 mV/dec lower than OTS devices, indicating a smaller voltage range transition from intrinsic to field-effect mobility in the OFET channel. In addition, SAM-treated devices exhibit an increase in the voltage range between V_T and their turn-ON voltage V_{to}. The increase in this voltage difference $|V_T - V_{to}|$ with SAM treatment has been reported previously[19] and is associated with an increase in the trap density at the dielectric/SAM interface,[33,34] which along with the interface dipole, contributes to the lower gate leakage in addition to the interface dipole. The trap density N_{trap} can be estimated as $N_{trap} = C_i|V_T - V_{to}|/e$ where C_i is the specific capacitance of the dielectric and e is the fundamental charge. The values of C_i for each of the three surfaces, shown in Table 2, are the average of twelve devices, fabricated with 50 nm gold contacts using the same shadow masks as for OFET source/drain electrodes. For bare oxide devices, we find a trap density $N_{trap,bare} = 4.9 \times 10^{10}$ cm^{-2}. By comparison, SAM-treated oxides yield trap values of $N_{trap,OTS} = 1.2 \times 10^{11}$ cm^{-2} and $N_{trap,FOTS} = 3.0 \times 10^{11}$ cm^{-2}. However, we caution that estimation of the trap density in the bare oxides, given their relatively large leakage currents and small potential differences $|V_T - V_{to}|$, may require a more comprehensive treatment of dopant gap levels in the thin oxide. It is reasonable to say that, at the very least, SAM treatment enables better estimation of the dielectric interface trap density.

Unlike in devices fabricated on thick oxides, the relatively high leakage in our OFETs precludes an analysis of the transistor channel conductivity that excludes the contribution of the gate leakage to the drain current. In Figure 4, we present the currents associated with the square-root transfer curves of Figure 3: drain (I_D), gate (I_G), and source (I_S). During these measurements, $V_D = 2$ V, and the gate was swept from −2 to +2 V. We see that, for n-SiOx transistors, in the OFF state the gate current I_G remained a factor of 2 higher than I_D and I_S. Upon reaching the threshold voltage at roughly −0.6 V, both I_D and I_S were larger than I_G by nearly 1 order of magnitude, with this difference becoming smaller as the gate voltage approaches 2 V (note that, near $V_D = 2$ V, the drain-gate voltage approaches zero as V_D increases). This decreasing difference in current is

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observed in the output curves of Figure 2, in which the OFETs fail to reach saturation due to increased leakage.

By comparison, both OTS- and FOTS-treated oxides exhibit OFF state currents I_S and I_G of comparable magnitude which are a factor of 5 larger than I_D. In addition, the value of I_G for the SAM-treated oxides is lower than for bare oxide devices. In the ON state, I_D and I_S are of the same magnitude and increase at a faster rate than I_G. This observation is consistent with the improved saturation behavior of the SAM-treated OFETs on n-SiOx. For p-SiOx devices, FOTS reduced leakage and improved saturation, while devices on OTS display larger I_G for negative gate bias. For both bare and SAM-treated oxide devices, V_T corresponds to the voltage at which the source-drain current increases rapidly relative to the gate current.

Due to the ∼1 eV work function difference between n-Si and Au, electrons accumulate at the oxide/NTCDI interface at equilibrium. Any additional negative surface charge on the oxide due to a SAM-dipole would serve to deplete electrons from the oxide + SAM/OSC interface. This effect manifests itself as an increase in the effective n-SiOx work function, moving further from vacuum toward that of p-Si. Comparison of the current characteristics of n-SiOx + FOTS and bare p-SiOx transistors in Figures 3 and 4 support this notion, as their currents and switching behavior closely resemble each other.

In the case of p-channel OFETs on an OTS- or FOTS-treated oxide, we expect to observe incremental accumulation of holes at the oxide interface, consistent with reports by Huang,[20] Chung,[12] Takeya,[35] and others. Our observations indicate that, while some gate leakage is reduced by simply adsorbing an alkyl to the oxide, the gate and subthreshold leakage decrease with increasing depletion in the channel due to the SAM dipole. As a result, we expect that reduction of leakage current using a dipolar SAM should be extendable to p-channel OFETs by employing a SAM with a positive dipole like aminotripropyl silane, which would deplete the channel of holes at the oxide/OSC interface.

Capacitance Measurements. Capacitance values for Si/oxide/Au and Si/oxide + SAM/Au structures are shown in Table 2. Deviations in these values from ideal thickness dependences may reflect variations in oxide thicknesses and are not important to the main conclusions of the paper. A more suitable metric that does not require the MIS-measured capacitance values is sheet transconductance, given by the mobility × capacitance product μC. This figure-of-merit has been used to compare performance of OFETs across various material and processing parameters.[13] Sheet transconductance, as well as threshold voltage V_T and μ_{meas}, was extrapolated from $I_D^{1/2}$ vs V_G plots using the saturation-regime equation for drain current in an FET: $I_D = \mu C(V_G - V_T)^2 W/2L$. Sheet transconductance is two times greater for OTS- and FOTS-treated devices on n-SiOx, while the transconductances are approximately equal for the three p-SiOx transistors. This increase in μC on SAM-treated n-SiOx reflects an enhancement of charge carrier accumulation, likely resulting from a reduction in carriers lost at the OSC/dielectric interface to leakage current. Notable for a single SAM layer on thin oxide, these transconductance values are comparable to reported multilayer SAM-on-native oxide OFETs.[36]

SUMMARY

These results demonstrate the effect of a molecular dipole as an electrostatic barrier, as well as the origin of a series contribution to the gate voltage, at the dielectric/OSC interface of an OFET. The selection of two SAMs of similar shape and length and different dipole magnitudes enabled a decoupling of the dielectric and dipolar contributions to OFET performance. Although both SAM treatments resulted in a more than 15-fold reduction in gate leakage current, the larger dipole of FOTS on n-type Si effected greater increase in the ON/OFF ratio and significantly reduced subthreshold leakage and swing. A comparison of OFETs on n- and p-type Si indicated that the tuning of the subthreshold leakage by dipolar SAMs may depend on the relative surface potential of the SAM with respect to its underlying substrate and may also include a contribution from the silane-oxide bonding itself. This work broadens the available electronic device properties that can be selectively tuned with inexpensive molecular layers. Moreover, the choice of a leaky oxide of marginal quality provided a platform on which to probe the utility of a molecular dipole for improving a poor dielectric. This surface engineering approach can be used to enhance other inorganic and polymer materials that may be considered unsuitable for electronic dielectrics.

EXPERIMENTAL SECTION

Oxides. Highly doped n-Si (As-doped) and p-Si (B-doped) wafers (SI-Tech, Process Solutions, $\rho = 0.001 - 0.005\ \Omega\cdot$cm) were sonicated in warm acetone and IPA and dried in a stream of dry nitrogen. Wafers initially had thermally grown 100 nm oxide layers. To obtain thinner layers, the original oxide layers were completely etched in a dilute 1:10 HF solution in deionized (DI) water and rinsed thoroughly in DI water prior to drying with dry nitrogen. Thin oxides were grown using a Technics PE II-A oxygen plasma system at 400 mTorr and 500 W for 2 min and placed in an oven in air at 200 °C for 2 h. Octyltriethoxysilane (OTS, also used to refer to the resulting layer on the oxide) and 1*H*,1*H*,2*H*,2*H*-perfluorooctyltriethoxysilane (FOTS) were used as purchased from Sigma Aldrich and stored in nitrogen at 4 °C when not in use. Self-assembly was achieved by placing 0.05 mL of each solution in a small scintillation vial centered within a 6 in. Pyrex crystallization dish containing several evenly spaced wafer pieces. Dishes were covered with aluminum foil and placed in a vacuum oven at 125 °C overnight under house vacuum at 45 cm Hg. Substrates were rinsed in hot toluene and dried with nitrogen prior to organic deposition.

Bare and SAM-treated oxides were characterized with X-ray photoelectron spectroscopy (XPS), ellipsometry, water contact angle, and atomic force microscopy (AFM). Carbon 1s spectra obtained via XPS shows an enhancement of the CH_2 bond at 284.5 eV for OTS, and FOTS samples show the double peaks at 291 and 293 eV with a ratio of ∼5:1, in agreement with the ratio of CF_2-CF_3 species[37] (Figure S5a, Supporting Information). Spectra of the Si 2p core electrons (Figure S5b, Supporting Information) for p-SiOx are at roughly 0.625 eV above those for n-Si, roughly equivalent to the expected workfunction difference between n-Si and p-SiOx.[32] Notably, we observed that, although the peak maxima for Si 2p and O 1s electrons in bare p-SiOx were also roughly 0.7 eV higher than in n-SiOx, these shifts were not observed in the p-SiOx + OTS or p-SiOx + FOTS surfaces.

The bare oxide thickness was measured by Brewster angle imaging ellipsometry (Accurion Nanofilm EP3) with 532 nm laser light, scanning between 55 and 85 degrees using a 5-point region-of-interest scan with n_{ox} = 1.462, and yielded a value of 11.5 ± 0.1 nm. Ellipsometric measurement of OTS and FOTS layers on oxide was obtained with a 5-point region-of-interest measurement using a multilayer model assuming the previous value of the oxide thickness, a range of 0.5 to 2 nm for the SAM thickness as a fitting parameter, and with $n_{SAM} = n_{ox}$, yielding monolayer thicknesses of 1.35 and 1.02 nm, respectively, with accuracy to within 0.1 nm. Static contact angles (Ramé-Hart) with deionized water droplets were 67.5° ± 2° for bare oxide, 88.7° ± 0° for OTS, and 100.5° ± 0° for FOTS, consistent with reported values in the literature for full coverage of these vapor-

deposited SAMs on silicon oxide.[37,38] The contact angle for our oxides, which is higher than the 28° angle generally observed for bare oxides, reflects the rough nature of our oxide surfaces. Images of bare and SAM-treated oxides were obtained with a Nanoscope V (Digital Instruments) AFM (Figures S6 and S7, Supporting Information).

OFETs. Active layers consisting of 40 nm of 8-2-Bn naphthalenetetracarboxylic diimide (NTCDI), synthesized in our laboratory (Figure 2b), were deposited at a rate of 0.2−0.4 Å/s in an Edwards thermal evaporation system at a base pressure below 3×10^{-6} Torr, at a substrate temperature of 75 °C. Gold contacts 50 nm thick were deposited at the same base pressure through shadow masks, at a rate of 0.3−0.6 Å/s, during which substrate temperature did not exceed 60 °C. With the exception of the HF etch and plasma oxidation, all processes were carried out in an ordinary (noncleanroom) environment using ACS reagent-grade solvents.

Each wafer type consisted of 12 devices, with three devices each of four different W/L ratios (80, 53.3, 40, and 32). All electrical characterization was performed on an Agilent 4155C Semiconductor Parameter Analyzer using a medium integration time (16.7 ms), under ambient fluorescent lighting conditions, in air. Si gates were scratched with a diamond scribe and contacted with Ga−In eutectic (Sigma-Aldrich). To prevent puncturing the thin oxide layers, devices were probed with low-resistance probes from Micromanipulator, onto which small (∼200 μm) drops of Ga−In eutectic were placed for contacting source and drain electrodes.

Surface Potentials. Several surface junctions were prepared for surface potential characterization using scanning Kelvin-probe microscopy (SKPM). For one set of samples, bare oxides were placed under vacuum for SAM attachment. After rinsing in hot toluene, substrates were patterned using S1813 photoresist (Microposit) on an EX620 UV aligner, and patterns were developed with trimethylammonium hydroxide (CD26, Microposit). The surfaces were placed in an oxygen plasma at 100 W for 60 s at a pressure of 400 mTorr to remove the SAM layer. The plasma power and time was chosen so as to not grow additional oxide on the exposed areas. Substrates were rinsed in acetone to remove the photoresist hard mark prior to SKPM characterization. For the second set of samples, bare oxide substrates were spin-coated with S1813 photoresist, patterned, and developed. Wafers were coated with an electron beam-deposited layer of Cr/Au (10 nm/50 nm, respectively) and left overnight in acetone for photoresist liftoff. Wafers were placed under vacuum for SAM treatment and rinsed in hot toluene for 2 h. Surface potentials were measured along the Au/oxide/Au and Au/oxide + SAM/Au interfaces. For the third set of samples, gold patterns with 150 μm linewidths were thermally evaporated (Edwards E306) at 10^{-6} Torr onto bare oxide substrates. Wafers were placed under vacuum for SAM treatment and rinsed in hot toluene for 2 h, followed by a hot bath of ethanol for Au liftoff from the oxide. Surfaces were then dried in a stream of nitrogen with a 0.22 μm filter and placed on a hot plate at 125 °C for 20 min prior to measurement. Surface potential measurements of oxide/oxide + SAM interfaces were carried out in air on a Veeco AFM using a NanoScope IIIa extender and a MultiTap-75G Cr/Pt tip (BudgetSensors) using a tip voltage of 2 V and a liftoff distance of 100 nm. Surface potentials for OTS- and FOTS-treated surfaces were 150−200 mV more negative than bare oxides, for both n-SiOx and p-SiOx.

ASSOCIATED CONTENT

Supporting Information

Additional device characteristics, surface morphologies, elemental analyses, and voltages. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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